

1998 Paper 5 Question 1

Structured Hardware Design

Describe individually or explain the differences between an FPGA (field programmable gate array) and a PAL (programmable array logic) device.

[10 marks]

Outline an implementation of a synchronous counter in both styles of programmable logic.

[6 marks]

What are the primary performance limitations when building large counters in each style of logic?

[4 marks]