1999 Paper 10 Question 7

Computer Design

Why is MIPS (millions of instructions per second) a poor measure of a computer's performance? [4 marks]

Explain why high-performance processors use pipelines to increase the MIPS rating and yet pipelines tend to increase the time to execute an instruction. [4 marks]

instruction fetch	decode/ register fetch	execute	memory access	register write back

With reference to the classic RISC pipeline above, explain what a data hazard is. [6 marks]

How are feed-forward paths used to reduce pipeline stalls? [6 marks]