

1999 Paper 7 Question 10

Specification and Verification II

Consider the following Verilog phrases:

```
initial r = 0;
always @(posedge clk) r = a + r;
```

Write down a formula in logic that relates `clk`, `a` and `r` at a level of abstraction where clock edges are explicitly represented. [4 marks]

Write down a second formula that models only the sequences of values of `a` and `r` at successive clock cycles. [4 marks]

Discuss the relationship between the two formulae. [4 marks]

Formalise and prove, using your second formula, that on the n^{th} cycle the value of `r` is the sum of the values of `a` on all the cycles up to the n^{th} . You may assume that values are natural numbers and ignore the possibility of overflow. [8 marks]