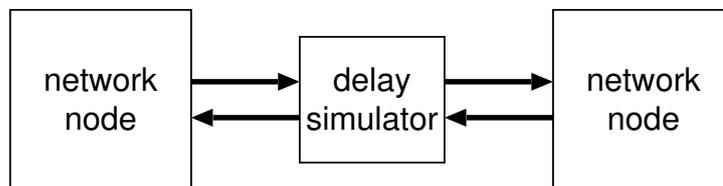


2000 Paper 2 Question 10

Structured Hardware Design

Some networking researchers wish to investigate the behaviour of a networking protocol when it is operating over long distance (high latency) links. To do this, they intend to build a *network delay simulator*, which they will use to interconnect a pair of network nodes. Operating concurrently on each link direction, the device will receive the data stream, delay it, then transmit it onwards to the other node.

The network uses a serial link operating at one gigabit per second, and the researchers require to be able to vary the delay such as to simulate links of between 1 and 5000 kilometres in length.



How much buffer memory is required to implement the device? [3 marks]

How can the data on the high-speed serial links be converted to a more manageable form? [4 marks]

Outline a design for the delay simulator, and hence address the following points:

- How many banks of memory does your design require, and what type(s) will be used?
- How will the control logic function, and what technology will it be built using?
- How will the delay inserted by the device be adjusted?

[13 marks]