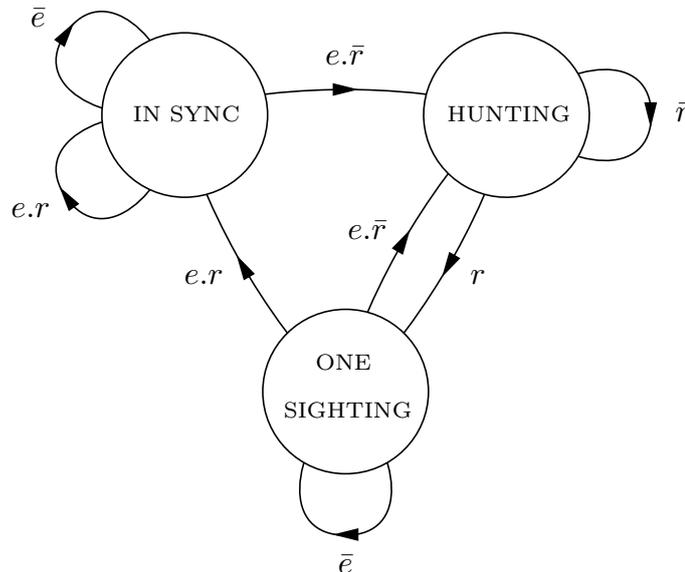


2000 Paper 2 Question 3

Digital Electronics

You are required to build a circuit whose inputs are a data input D and a clock C . The data input D is used to pass a stream of bits into the circuit. Every 64 bits, an 8-bit synchronisation pattern 01100110 appears in the stream, followed by 56 bits of changing information.

- (a) Design a combinational circuit incorporated with an 8-bit shift register that recognises the synchronisation pattern and asserts a signal r for 1-bit time whenever the pattern appears. [5 marks]
- (b) The pattern 01100110 may of course appear in the changing information bits. Thus we must have some means of remembering if we are in sync so that we can expect the 01100110. Let us use the following state diagram, where e (expected) will be true whenever we expect to see r true.



Explain what each of the states is for and implement the finite state machine described in the diagram, including the equation of s which is true while the machine remains in synchronisation. [10 marks]

- (c) Explain briefly how the signal e might be produced. [2 marks]
- (d) Another output, the byte clock b , is to have a low to high transition every eight bits, with one such transition occurring when an expected synchronisation pattern appears in the shift register (and then eight bits later, etc.). Explain how this signal might be produced. [3 marks]