2001 Paper 8 Question 2

VLSI Design

(*a*) The *constant field* model of MOS scaling applies a dimensionless factor α to manufacturing dimensions (length, width and thickness), voltages and processing concentrations, so that channel thickness remains unchanged. For example, with $\alpha = 1$, the dimensions are unchanged; with $\alpha = 2$, they would be halved. Derive approximate expressions for the consequent scaling of

- gate area
- channel resistance
- current
- load capacitance
- gate delay
- static power consumption (per gate)
- power density (per unit area)
- current density (in wires)

What are the main implications for speed, size and power? [8 marks]

(*b*) *Constant voltage* is an alternative model in which the only manufacturing dimensions are scaled, leaving voltages unchanged, so the channel thickness increases by a factor α. Derive approximate expressions for the consequent scaling and summarise the main implications. [8 marks]

(*c*) What further factors make both models inappropriate as device sizes continue to decrease? [4 marks]