# 2002 Paper 8 Question 2

## VLSI Design

(*a*) Draw a transistor-level circuit diagram of a 2-input NAND gate in CMOS and describe its operation. [6 marks]

(*b*) Sketch a stick diagram and physical layout for the same gate, paying attention to the dimensions of the transistors to ensure balanced rise and fall times. [6 marks]

(*c*) Draw a transistor-level circuit diagram of a 2-input Muller C-element and describe its operation. Why is this sometimes described as an AND gate for events? [8 marks]