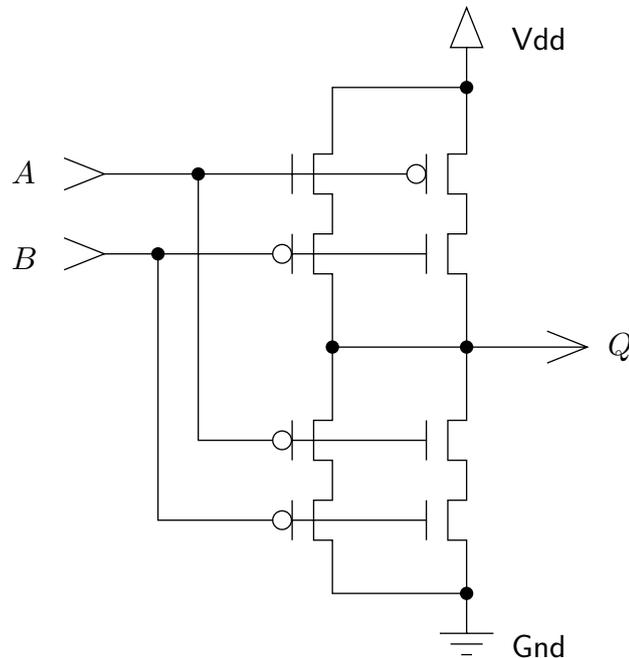


## 2003 Paper 8 Question 2

### VLSI Design

The designer of a CMOS standard cell library has proposed the following circuit for an XOR gate:



Explain how the circuit operates. [2 marks]

Although the circuit appears digitally correct, it operates slowly. Moreover, when two of the XOR gates are cascaded to calculate the XOR of three signals, the results are unreliable. Suggest explanations for these two problems. [4 marks]

Propose a modification to the circuit which retains the general design but introduces two pairs of additional inverters to address the problems. [4 marks]

Another designer cascades two of the revised gates as part of a full adder, and observes that the resulting circuit is large and slow. Extend the design to provide the XOR of three inputs directly. Compare its size and speed with the cascaded version. [5 marks]

Yet another designer is working on an asynchronous design and needs a two-input XOR gate for dual-rail logic. Sketch a design which ensures that all the input signals become valid before any output does so, and that all the inputs become clear before any outputs do so. [5 marks]