2006 Paper 7 Question 7

Specification and Verification II

(*a*) What are Binary Decision Diagrams and how are they used to represent state-transition functions symbolically? [4 marks]

(*b*) What is temporal abstraction? How are models at different temporal abstraction levels related? [4 marks]

(*c*) What is the difference between LTL and CTL? [4 marks]

(*d*) How do the Verilog and VHDL simulation cycles differ? [4 marks]

(*e*) What is the difference between formal verification using model checking and using theorem proving? [4 marks]