

2007 Paper 12 Question 2

Computer Design

- (a) What is the difference between the *latency* and the *bandwidth* of a communication link? [2 marks]
- (b) Why are control-flow processors sensitive to memory latency even if the memory bandwidth exceeds what the processor could ever require? [4 marks]
- (c) How is average memory latency typically reduced? [5 marks]
- (d) What is the difference between serial and parallel communication and what is the receiver required to do to recover the data in each case? [5 marks]
- (e) The PCI communication standard for add-on cards for PCs has moved to PCI express (PCIe). PCI uses a parallel bus to communicate to several cards whereas PCIe uses sets of point-to-point serial links for communication. Why are multiple serial links rather than parallel buses preferred for high bandwidth communication? [4 marks]