2007 Paper 7 Question 11

VLSI Design

(*a*) Sketch a transistor-level circuit for a 2-input AND gate in static CMOS. [2 marks]

(*b*) Consider the design of a 16-input AND gate in static CMOS.

(*i*) Explain why the 2-input design could not simply be scaled up. [2 marks]

(*ii*) Sketch alternative designs using two and four levels of NAND and NOR gates. [2 × 2 marks]

(*iii*) Use logical effort to estimate the delay of both the designs, assuming that the conducting channel in a pFET has twice the resistance of that in an nFET. [10 marks]

(*iv*) Determine the approximate value of the electrical effort at which their speeds are equal. [2 marks]