COMPUTER SCIENCE TRIPOS Part II – 2012 – Paper 8

3 Comparative Architectures (RDM)

(*a*) Two independent threads are run on different processors in a chip-multiprocessor. Each thread simply increments a private counter one million times. The two counters are stored in consecutive memory locations. It is discovered that running the threads sequentially is faster than running them in parallel. What may cause this type of behaviour? [5 marks]

(*b*) Cache coherence protocols are classified as either invalidate or update protocols. What are the potential advantages and disadvantages of adopting an update rather than an invalidate protocol? [5 marks]

(*c*) Sequential consistency offers a simple and intuitive memory consistency model. Why is sequential consistency rarely supported by modern chip-multiprocessor designs? [5 marks]

(*d*) What information does the directory provide in a directory-based coherence protocol? [5 marks]