

COMPUTER SCIENCE TRIPOS Part II – 2013 – Paper 8

3 Comparative Architectures (RDM)

- (a) How do superblock and trace scheduling differ? [4 marks]
- (b) How might a programmer improve the performance of a program given detailed knowledge of a processor's memory hierarchy? [6 marks]
- (c) Larger scale networks, i.e. those involving chip-to-chip or longer distance communications, have been designed for many years. What new challenges and constraints are introduced when designing on-chip networks? [6 marks]
- (d) As fabrication technologies scale the performance of wires improves slowly relative to that of transistors. Why is this particularly problematic when attempting to increase the performance of superscalar processors? [4 marks]