COMPUTER SCIENCE TRIPOS Part II – 2014 – Paper 9

11 System-on-Chip Design (DJG)

(*a*) A mobile phone uses an average power of 20 mW when not in use. Given that its battery voltage is 3V with capacity 500 mAh, what is the maximum interval between rechargings? [2 marks]

(*b*) The supply regulator converts the battery voltage to a 1 Volt supply for the digital logic and is 80% efficient. If the phone dissipation during a CPU-bound computer game is 3 Watts and the processor clock frequency is 500 MHz, what, roughly, is the average track capacitance discharged each clock cycle? State any assumptions. For instance, you might assume that the screen backlight dissipates 1 Watt. [3 marks]

(*c*) What are the main differences, in terms of latency, throughput, capacity and energy use, between an on-chip register file and an off-chip RAM? [4 marks]

(*d*) Simulation in advance of manufacture can provide an estimate of power consumption. Explain what power estimation procedures might be used when simulating at each of the following design stages:

(*i*) A TLM model of the SoC that is running the production software.

(*ii*) A Verilog RTL model of the complete SoC prior to gate synthesis.

(*iii*) A Verilog netlist of the complete SoC prior to placement.

(*iv*) A Verilog netlist of the complete SoC after place and route.

[8 marks]

(*e*) A design goal for the phone is, "The battery life on standby shall always be greater than three days." Discuss whether this is a safety or liveness assertion and where it might best be embodied in the design flow. [3 marks]