COMPUTER SCIENCE TRIPOS Part II – 2015 – Paper 8

1 Comparative Architectures (RDM)

A multicore processor consists of eight scalar cores. Each core has private 8KB L1 instruction and data caches. The cores are supported by a 4MB L2 cache that is 8-way banked. Communication between the cores and the L2 cache banks takes place over two crossbar switches (one for communication in each direction). The L2 cache maintains a directory that shadows the L1 tags. The L1 caches are write-through, with allocate on load and no-allocate on stores.

(*a*) Describe a simple cache coherence protocol suitable for this processor. [8 marks]

(*b*) In the simple scheme you have described, what states may L1 cache lines be in? [2 marks]

(*c*) Why might it be better to shadow the L1 tags rather than adding state to each L2 cache line? [5 marks]

(*d*) What advantages does your protocol have over a simple snooping coherence protocol running over a shared bus? [5 marks]