COMPUTER SCIENCE TRIPOS Part IA – 2025 – Paper 2

1 Digital Electronics (ijw24)

(*a*) Show algebraically that the following functions can be implemented using either a 2-input exclusive OR gate or its complement.

(*i*) $F(X, Y) = X.Y \oplus (X + Y)$

(*ii*) $G(A, B) = A \oplus B \oplus (A + B) + \overline{A}.\overline{B}$

[4 marks]

(*b*) (*i*) Show how the following function may be implemented using an AND gate, an OR gate and an XOR gate, all having two inputs.

$$H(A, B, C, D) = \overline{A}.C + \overline{A}.D + \overline{B}.C + \overline{B}.D + A.B.\overline{C}.\overline{D}$$

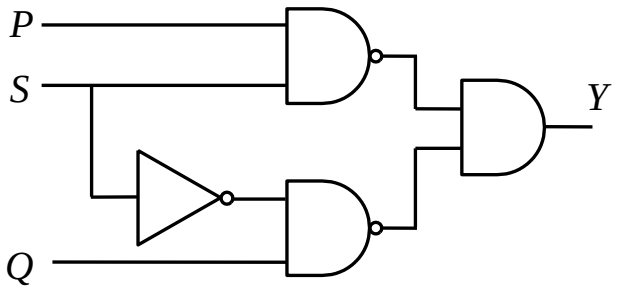
[3 marks]

(*ii*) Show how the function in Part (*b*)(*i*) may be implemented using a 16:1 multiplexer. Use variable A as the most significant bit of the multiplexer control inputs. [2 marks]

(*iii*) With the aid of a truth-table, show how the function in Part (*b*)(*i*) may alternatively be implemented using an 8:1 multiplexer and a NOT gate. Use variables A, B and C as the control inputs, where A is the most significant bit. Assume that complemented input variables are *not* available.

[4 marks]

(*c*) For the following circuit, assume that all the logic gates have an equal value of *non-zero* propagation delay and that $P = 1$ and $Q = 1$



(*i*) Describe what happens at output Y when input S changes from 1 to 0.

(*ii*) Show how the undesirable change observed at Y in Part (*c*)(*i*) may be removed.

[7 marks]