COMPUTER SCIENCE TRIPOS Part IB – 2025 – Paper 5

7 Introduction to Computer Architecture (rdm34)

(*a*) Why might having a formal description of an Instruction-Set Architecture (ISA), for example, for the RISC-V ISA, be useful? [4 marks]

(*b*) In order to achieve the benefits of pipelining it is necessary to balance the delay of logic in different stages. What might make this difficult or expensive to achieve? [4 marks]

(*c*) Why are FPGAs not commonly used for high-volume markets? [4 marks]

(*d*) We run timing analysis after logic synthesis and a particular critical path is reported. We now place and route our design and a different critical path is identified. Why might this happen? [4 marks]

(*e*) After manufacturing our design, we discover that it experiences significant clock skew, meaning the clock signal reaches different flip-flops at different times due to an issue in the clock tree's design. What are the two potential problems this skew could cause? In each case, describe any steps that can be taken to mitigate the issues in the *manufactured* chips even if they result in reduced performance. [4 marks]