COMPUTER SCIENCE TRIPOS Part II – 2025 – Paper 9

1 Advanced Computer Architecture (rdm34)

(*a*) Conventional instruction sets specify an instruction's operands by using register names. We could alternatively specify an instruction's operands by inter-instruction distance, that is, indicating the required operand by counting backwards to the instruction that generated it.

(*i*) Describe one possible advantage of this approach. [3 marks]

(*ii*) If we specified an instruction's operands in this way we could still retain the register file. Describe a simple way to determine the destination register for each instruction that would mean it would not be encoded in the instruction. [3 marks]

(*iii*) In what cases would it be difficult to specify operands using the scheme described? [6 marks]

(*b*) Precisely what invariants does a cache coherence protocol guarantee? [3 marks]

(*c*) Imagine a multi-core system with a directory-based cache-coherence protocol.

(*i*) What are the benefits of a directory-based cache coherence protocol over a snooping protocol? [2 marks]

(*ii*) Why might an L3 cache have more tags and directory entries than cache lines, that is, be a non-inclusive cache that maintains an inclusive directory? [3 marks]