Formal Verification of Analog Circuits in the Presence of Noise and Process Variation

Rajeev Narayanan[1], Behzad Akbarpour[1], Mohamed H. Zaki[2], Sofiène Tahar[1] and Lawrence C. Paulson[3]
[1]Dept. of Electrical and Computer Engineering, Concordia University, Montreal, Quebec, Canada
Email: {r_naraya, behzad, tahar}@ece.concordia.ca
[2]Dept. of Computer Science, University of British Columbia, Vancouver, British Columbia, Canada
Email: mzaki@cs.ubc.ca
[3]Computer Laboratory, University of Cambridge, Cambridge, UK
Email: lp15@cam.ac.uk

***Abstract*—We model and verify analog designs in the presence of noise and process variation using an automated theorem prover, MetiTarski. Due to the statistical nature of noise, we propose to use stochastic differential equations (SDE) to model the designs. We find a closed form solution for the SDEs, then integrate the device variation due to the *0.18μm* fabrication process and verify properties using MetiTarski. We illustrate the proposed approach on an inverting Op-Amp Integrator and a Band-Gap reference bias circuit.**

I. Introduction

In recent years, advanced technologies have allowed designers to develop smaller, faster, low power integrated analog/digital/RF designs in a single chip, known as systems-on-a-chip (SoC). With this complex integration among various blocks and due to non-linear dynamics of analog/RF designs, effects like inheritance or interactive noise [10] and deep-submicron process such as *photomasking, diffusion, ion implantation, oxidation,* and *epitaxial growth* have influenced the quality and yield of the manufactured circuits [3]. For designers, the challenging questions are *how do noise and process variation influence the behavior of analog designs?* And *how to choose the appropriate noise model and integrate process variations in the verification environment?*

Current circuit simulators for statistical analysis of noise that involve studying the power spectral density can suffer from memory space problems [8] due to increases in higher order harmonics. Due to the statistical nature of the noise, we are interested in finding a statistical solution in continuous-time rather than a detailed response of the system, therefore we propose to use stochastic differential equations (SDE) [4] as an analog noise model. In addition to noise, the effect of process variation are evaluated using *Worst Case* or *Monte-Carlo* methods [3] in circuit simulators. The former provides a fast simulation technique for a single device performance (e.g., speed, power, area) but may increase the design efforts and costs. In contrast, Monte-Carlo methods take into account a predefined distribution (usually normal distribution) of the device parameter due to process variation.

We [12] incorporated SDE based methodology for monitoring properties in the presence of noise and process variation. The approach is based on modeling the noise using SDEs and numerically simulating, in MATLAB, and monitoring the property of interest. We showed that properties that are satisfied without noise, have failed in the presence of noise, thereby proving the method to be efficient in finding bugs. Though attractive, such simulation based methods lack the rigor to ensure the correctness of the design. In the recent years, statistical based model checking [6] has been successfully used to verify the saturation property in a simple analog circuits, such as a third-order $\Delta\Sigma$ modulator. Model checking techniques are still in their infancy and no model checker exists today that could be used to verify noise with process variation for analog circuits. Moreover, it is well known that for large circuits model checking can easily run into state-space explosion. By contrast, formal methods in particular, theorem proving can deliver the highest level of assurance for verification [5]. Akbarpour and Paulson [2] have very recently proposed an automatic proof procedure for inequalities on elementary functions, called MetiTarski, which we will adopt in this paper. MetiTarski has been lately used [13] to verify properties concerning oscillation and the change in gain due to component tolerances for analog circuits. In this paper, we modify that approach to address the issue of noise and process variation.

MetiTarski combines a resolution theorem prover with a set of axioms and a decision procedure to automatically prove elementary functions such as sine, cosine, exp, log, etc.,. In general, MetiTarski turns a verification property, in the form of a first-order formula, into an inequality over special functions. Proofs are typically found in a few seconds and can be checked separately for the correctness of the results. As most of the closed form solutions in an analog circuit involve elementary functions it is intriguing to study the effect of noise using MetiTarski. However, the challenge is to incorporate the above technique for noise verification in the presence of process variation using SDEs.

In this paper, we propose an SDE based verification methodology in a theorem proving environment using MetiTarski. Our approach is illustrated on an inverting Op-Amp Integrator and Band-Gap reference bias circuit.

II. Stochastic Differential Equation

An SDE is an ordinary differential equation (ODE) with a stochastic process that can model unpredictable behavior of any continuous systems [4]. The random term in an SDE can be purely additive or it may multiply by some deterministic term. For example, consider the population growth model described by the following differential equation

$$\frac{dN}{dt} = a(t)N(t); \quad N(0) = A \tag{1}$$

where *N(t)* and *a(t)* are, respectively, the size of the population and the relative rate of growth at time *t*, and *A* is some initial constant. *a(t)* is unknown and random, hence a reasonable mathematical interpretation of the randomness for the above equation can be described as

$$\frac{dN}{dt} = a(t)N(t) + \xi_t N(t); \quad N(0) = A \tag{2}$$

The term *a(t)N(t)* is the deterministic drift coefficient while the term $\xi_t N(t)$ represents the stochastic effect [4]. However, in SDE terminology, the above equation can be represented in two forms [4]: *Itô* or *Stratonovich* form. If we consider ξ_t to be the pathwise derivative of *Brownian* motion [4] (or *Wiener* Process [4]) dB_t, then Equation 2 can be written in *Itô* differential and integral form as

$$\begin{aligned} dN &= a(t)N(t)dt \quad &+N(t)dB_t \\ N &= \int_0^t a(s)N(s)ds \quad &+\int_0^t N(s)dB_s \end{aligned} \tag{3}$$

To solve Equation 3, traditional calculus lacks the infrastructure to handle a stochastic process, and hence we need special mathematical interpretation in the form of stochastic calculus to solve the equations involving Brownian motion [4].

III. Proposed Methodology

Figure 1 shows the proposed methodology for modeling and verification of analog designs in the presence of noise and process variations using the automated theorem prover MetiTarski. Thereafter, given an analog design described as a system of *ODEs*, the idea is to include a stochastic process that describes the noise behavior. Since there are no functions/procedures that can automatically incorporate stochastic processes, we manually generate the *SDEs* of the form described in Equation 3. The current methodology can handle linear SDEs, meaning, a time-invariant design that operates under small-signal conditions with a fixed operating point. Though, there are some tools that can solve simple linear SDEs, most of the real-world problems have to be solved manually using stochastic calculus.

Based on the process variation, technology vendors created a library of devices with different process corners such as *slow, nominal* and *fast* [14]. Each process corner characterizes the device in terms of power consumption, speed, area, etc., thereby allowing the designers to choose from a range of devices based on the application and design requirements. Based on the type of process, various design parameters in the circuit are calculated for different process corners. These values are included as a design parameter to get the closed form solution.

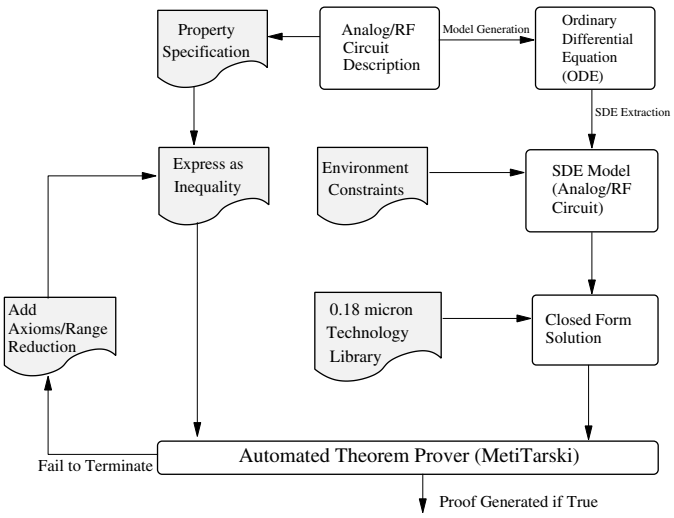

Fig. 1. SDE based Verification Methodology using MetiTarski.eps

For environment constraints, this may include the amplitude of the noise, initial conditions of the circuit current and voltages. The environment constraints are passed as a parameter to the SDE model to get the closed form solution. The closed form solution allows us to express the properties of interest as inequalities over special functions along with axioms. These axioms provide MetiTarksi with the type of clauses to use when performing the special function to polynomial substitution. The resulting axiom set replaces inequalities concerning those functions by algebraic inequalities.

If MetiTarski is successful in proving the inequality, it delivers a proof script and we are done. If unsuccessful, it will run until terminated by the user. Additional axioms are then added or removed in formulating a proof. There are certain axioms that are available for special functions that take on extreme values. Including them unnecessarily in proofs will increase the computation time. If still unsuccessful, *range reduction* is applied to the trigonometric functions to further eliminate any extreme values that can cause problems for MetiTarski's decision procedure.

IV. Applications

Amplifiers, integrators and mixer circuits are considered to be the core blocks for many analog designs. For illustration purposes, we have applied the proposed methodology on an inverting Op-Amp Integrator and a Band-Gap reference circuit. The experiments were performed on a ULTRA SPARC (177 MHz CPU, 1GB memory). Refer [11] for more applications.

A. Non-Ideal Op-Amp Integrator [8]

One of the practical limitations of Op-Amps occurs due to unbalance in their internal transistors and resistors. To account for this in a circuit design, the mismatch is modeled as an offset voltage, V_{OS}, in series with op amp's input terminals as shown in Figure 2.

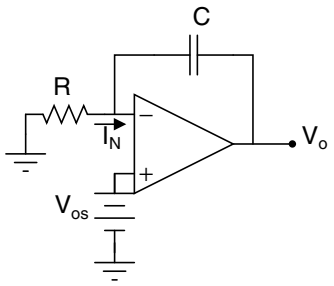

Fig. 2. Inverting Op-Amp Integrator [8].

The inverting Op-Amp integrator can be described as

$$C\frac{dV_o}{dt} = -\left[\frac{V_{OS}}{R} + I_N\right] \tag{4}$$

Assuming a white noise process at the offset voltage source V_{OS}, Equation 4 can be rewritten to incorporate randomness as given by

$$dV_o = -\frac{1}{C}\left[\frac{V_{os}}{R} + I_N\right]dt + \sigma\xi(t) \tag{5}$$

where $\xi(t)$ represents an independent white noise processes, and σ describes the amplitude of the noise. Equation 5 represents an *Itô* SDE in differential form. In the above equation, the first term is the deterministic part, which describes the trajectory of the output process without noise, and the second term is the stochastic part, which modifies the output trajectory due to noise. Our aim is to extract information such as mean *E[V_o]* and variance *Var[V_o]*, because the mean represents the output trajectory in the absence of noise and the variance gives the amount of deviation due to noise. Now, the goal is to find a closed form solution using stochastic calculus and the following equations summarize the mean and variance for the inverting Op-Amp integrator.

$$\begin{aligned} E[V_o] &= -\frac{1}{C}\left[\frac{V_{OS}}{R} + I_N\right]t \\ Var(V_o) &= \sigma^2 t \end{aligned} \tag{6}$$

Equation 6 represents the closed form solution of the inverting Op-Amp integrator. The next step is to formalize and verify circuit correctness properties for a given set of parameters and input source in the presence of process variation.

Property Observation: $[t \leq 15e-6]$
One important property, for a given set of parameter values: *how long will it take for the output V_o to saturate after the power is turned on?* The behavior in question is stated as the bounded safety property. For the property to be satisfied for the variation of resistance and capacitor, the time *t* taken by the output voltage V_o to saturate to a value of *15V* should be $\leq 15\times^{-6}$. Please refer [11] for parameter values.

For a *0.18μm* CMOS technology, we have to account for 15 to 25% variation in sheet resistance in order to study the effect of process variation [14], i.e., the sheet resistance R_{sh} is 7.9$\Omega/\square$ [1]. This means that, for the process corners, the variation in R_{sh} would be 15%, 20% and 25%, respectively [14]. Typically $\pm$20% variation is taken for capacitance due to *0.18μm* process [7].

The first-order formula of the above property is described in MetiTarski syntax as

```
fof(
Integrator,conjecture, ! [R, C] :
( (9*10^3≤R & R≤11*10^3 & 80*10-12≤ C & C≤120*10^-12)
  => (15*R*C/(-0.0015+R*0.0001001))
  ≤ 15*10^-6)).
```

where 'fof' indicates that the inequation is a first-order formula. It is followed by a label name, i.e., it is *Integrator*, and a keyword "$conjecture$" indicating that the following formula is to be proved with the included axioms. $9 \times 10^3 \leq R$ *&* $R \leq 11 \times 10^3$ represent the variation in the resistor, $80 \times 10^{-12} \leq C$ *&* $C \leq 120 \times 10^{-12}$ represent the variation in the capacitor due to *0.18μm* process for *slow, nominal* and *fast* process corners. The above formula can be read as follows: For All (!) *[R, C]* between $9 \times 10^3 \leq R$ *&* $R \leq 11 \times 10^3$ *&* $80 \times 10^{-12} \leq C$ *&* $C \leq 120 \times 10^{-12}$, the formula which represents the saturation time of the output voltage is always $\leq 15 \times 10^{-6}$ sec. MetiTarski is able to prove the above formula, verifying the property.

B. Band-Gap Reference Bias Circuit

For any biasing circuit, one of the most important performance issue is its dependence on temperature. The variation in temperature attributes to the fractional change in the output voltage/current, thereby affecting the functionality of the design [8]. Figure 3 shows a BJT based reference generator biasing circuit, for which we are interested in knowing *how the variation of noise with respect to temperature affects the behavior of the circuit.*

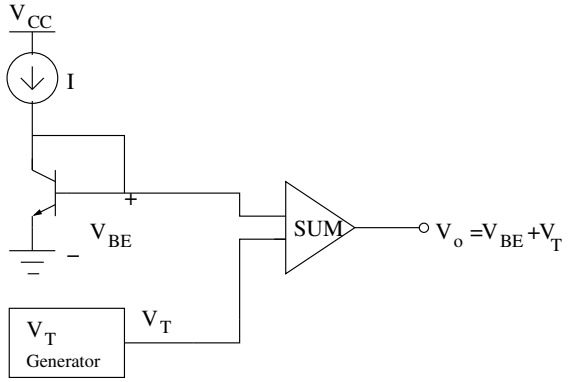

Fig. 3. Band-Gap Reference Circuit [8].

Assuming a temperature varying noise process at the voltage source V_T, the behavior of the circuit can be written as [8]:

$$\frac{dV_o}{dT} = (\gamma - \alpha)\frac{V_T}{T}\left(\frac{T_0 - T}{T}\right) + \frac{(\gamma - \alpha)(T_0 - T)}{T^2}\xi(T) \tag{7}$$

where γ and α are temperature independent constant and *T* is

the temperature. Solving for expectation and variance, we get

$$\begin{aligned} E[V_o] &= (\gamma - \alpha)V_T \left[-\frac{T_0}{T} - \ln(T) + \ln(T_0) + 1 \right] \\ Var(V_o) &= \left[\frac{T_0}{T^2} - \frac{T_0^2}{3T^3} - \frac{1}{T} + \frac{1}{3T_0} \right] \end{aligned} \tag{8}$$

where T_0 is the temperature at which the output temperature coefficient is zero. Equation 8 represents the closed form solution of V_o due to temperature varying noise source. The next step is to formalize and verify circuit correctness properties for a given set of parameters and input source.

Property Observation: $[V_o \geq 3.13mV]$
The property of interest is: *whether for the given set of parameters and variation in temperature T, will the output voltage V_o is greater than certain threshold voltage?* Since manufacturing techniques for BJT are different from those of CMOS, the effect of process variation for BJT's are not considered. Refer [11] for parameter values.
The first-order formula of the above property is described in MetiTarski syntax as

```
fof(
Ref_Gen,conjecture, ! [T] :
( (300≤ T & T ≤400)
  => 0.0572*(5.018+(411/T)-(ln(T/100)+ 4.605170186))
  + 0.0572*(((411/(T^2))-(56307/(T^3))
  * (1/T)+ 0.811*10^(-3)))
  ≥ 0.00313)).
```

The above formula can be read as follows: For All (!) *[T]* between $300°K \leq T \;\&\; T \leq 400°K$, the formula which represents the variation of output voltage is always ≥ 0.00313 Volts. The property is proved with scaling of the *ln* function in order to bring the argument of the *ln* function into a region where the bounds are more accurate.

C. Discussion

By turning the verification property into an inequality over special functions, MetiTarski is able to prove the property of interest in the presence of noise and process variation of the above circuits. We obtain formal proofs that can also, with perseverance, be checked by humans to increase confidence that the design correctly matches its specification. Since the formula for the inverting Op-Amp integrator involves only polynomial functions, we did not face any problem with MetiTarski, and it took *3.52 sec* to run the proof. However, for the Band-Gap reference bias circuit, MetiTarski failed to terminate initially because the *ln* function tends to be out of bounds. By using a scaling approach, we were able to prove the property in *8.58 sec*. In summary, as MetiTarski is a proof based analysis, this process is much more reliable than manual inspection (visual or textual) of simulation traces, which does not guarantee the correctness of the design.

V. Conclusion

In this paper, we have presented a verification methodology based on automated theorem proving for noise and process variation in analog designs. Our approach is based on modeling the noise using SDEs, finding a closed form solution and then integrate the device variation due to the *0.18μm* fabrication process for proving properties using MetiTarski. We have demonstrated that the methodology can be applied to a certain class of analog circuits. The main advantage of the methodology is that it yields a complete proof with logical inference steps that can even be inspected manually, thereby providing confidence during the design development.

The proposed methodology is limited to linear time-invariant designs. For non-linear circuits, a closed form solution for the SDEs might not exist. Also, such analytical expressions have created an imbalance with the initial circuit description in terms of accuracy. Hence, we are investigating numerical solutions [9] of the SDEs with error bounds and use MetiTarski to prove properties. While there are many numerical techniques available for SDE analysis, there is a need to test the numerical models for accuracy, speed and stability, and to decide on the appropriate ones for practical applications. The proposed methodology involves several manual steps. It is our intention to automate some of these in the future.

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